Frank Li

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Education

University of Washington – Seattle, B.S. Computer Science (GPA: 3.9) Graduation: Spring 2026

Courses: Data Structures and Parallelism, Algorithms, Modern Algorithms, Distributed Systems, Datacenter Systems, CV, NLP, ML, AI, Deep Learning, FPGA Design, Compilers, Operating System, Linear Algebra, Numerical Analysis, Linear Optimization, Systems for ML

Technical Skills

Languages: Python, Java, Kotlin, C, C++, HTML, CSS, Javascript, Typescript, Shell, SQL, Go, SystemVerilog, Rust, OCaml, LaTeX
Frameworks: Node, React, Tailwind, Next, gRPC, tRPC, Prisma, Jest, AWS SDK/CDK, Spring, Boost, NumPy, Pandas, PyTorch, Tokio
Tools: Linux, Git, CMake, PostgreSQL, AWS, Docker, Kubernetes, ModelSim, Quartus, FPGA, Serverless, GDB, Valgrind

Experiences

NVIDIA Fall 2025
Incoming System Software Engineer Intern - ML Ops Santa Clara, CA

Two Sigma Summer 2025
Incoming Software Engineer Intern New York, NY

Amazon Jun 2023 – Present
Jr. Software Development Engineer III (Year-round SDE intern) Seattle, WA

- Developed **dozens of new features** for our tier-1 content management service with **millions of enterprise users** using **Java and AWS**.
- Improved user privacy and experience by **automating end-to-end data encryption and asset regionalization, reducing latency by 20%**.
- Architected an **edge-optimized** web app with CDN caching, serverless backend, and **reusable infrastructure-as-code with AWS CDK**.
- Led the restructuring of data models and **utilized concurrent asynchronous queries** to **reduce query times by 40%** for our customers.

UW High-Performance and Data-Intensive Computing (HPDIC) Lab Jan 2024 – Jun 2024
Undergraduate Researcher (Vector Databases) Seattle, WA

- Formulated **two new multi-vector search query algorithms** based on hierarchical navigable small-world and custom distance metrics.
- Extended pgvector (PostgreSQL vector extension with **9.8k Github stars written in C**) to support semantic multi-vector queries.
- Developed a **Python client** to interface with pgvector, then ran **performance benchmarks on high-performance compute clusters**.

Shanghai Media Intelligence Technology Jul 2021 – Aug 2021
Software Engineer Intern Shanghai, China

- Developed a presentation tool with React that compares high-throughput video streams with **timestamp synchronization and caching**.
- Enhanced the data pipeline by **implementing additional automation and data augmentation, increasing model accuracy by 5%**.

Creative Hose Equipment Technology Jul 2018 – Aug 2018
Fullstack Developer Intern Beijing, China

- Developed tools for supply line inventory management using **Java with Spring Boot, Hibernate, and JSP with Oracle database**.
- **Secured data operations** by utilizing prepared statements and serializable transactions to prevent SQL injection and race conditions.
- Spearheaded the transition to **embedded PWA** by creating a prototype, **improving performance and increasing adoptability by 40%**.

Projects

Cloud VM CPU Cache Latency Analyzer | *C++, Python, GCP, Shell, Pandas, Seaborn*

- Leveraged **C++ multithreading, atomics, and syscalls** to set threads' CPU core affinities, analyzing **latency of cache coherent operations**.
- Presented the read and write latencies between each cores on a heatmap, identifying CPU core pairings that **reduce latencies by 80%**.

Dockerized Yelp Clone with Performance Analysis | *Go, Lua, gRPC, Protobuf, Docker, Kubernetes, Shell, GCP*

- Architected a Yelp clone with dockerized microservices in **Go**, utilizing **gRPC** for communication and **Kubernetes** for orchestration.
- Coded **Lua scripts with wrk2** to benchmark the system and **identify bottlenecks**, then implemented caching to **reduce latency by 30%**.

Data-Driven Stock Vetter | *Python, Javascript, FastAPI, BeautifulSoup, GPT-3.5, LSTM, K-Means*

- Implemented **k-means clustering** to sample unique news across multiple web sources, passing it as context to prompt **GPT-3.5**.
- Trained an **LSTM** for rating stocks, displaying the results along with the GPT-3.5 responses and stock trends on a React website.

FPGA Dance Dance Revolution | *SystemVerilog, Intel Quartus, ModelSim, FPGA (DE1-SoC)*

- Prototyped a DDR game on an **FPGA in SystemVerilog**, implemented **FSMs like D-flip-flops, clock divider, and LFSRs** with unit tests.
- Utilized **Quartus** to synthesize the design and interface with hardware peripherals, and **ModelSim** to simulate and debug module states.